Abstract

The present invention relates to a method and system for performing a data transfer between a shared memory (16) of a processor device (10) and a circuitry (20) connected to the processor device (10), wherein the data transfer is performed by triggering a DMA transfer of the data to the processor device, adding the DMA transfer to a transaction log, and providing the transaction log to the processor device, when the transaction log has reached a predetermined depth limit. The processor device is then informed of the DMA transfer of the transaction log, so as to be able to validate the transferred data. Thereby, significant background data movement can be provided without introducing high core overheads at the processor device (10).

[Fig. 1]